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Super-threshold computing and performance variations of FinFET single-rail current mode logic circuits[1]

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Abstract. Lowering the supply voltage of FinFET Current Mode Logic (CML) can achieve low power-delay product (PDP). This paper presents super-threshold computing of FinFET Single-Rail CML (SRCML) circuits to attain low PDP and performance variations in super-threshold regions. A full-adder was implemented to verify their power efficiency. The two-input NANDs based on FinFET SRCML, FinFET DRCML (Dual-rail MCL), and static complementary FinFET logic were investigated in terms of probability distributions of propagation delay in different source voltages. The results show that the power consumption of super-threshold FinFET SRCML circuits can be reduced compared with the normal supply voltage without performance degrading and accepted performance variation penalty.

Key words. Super-threshold computing, performance variation, FinFET current mode logic.

1. Introduction

High-speed circuits are now required in a wide range of applications such as high-speed CPU and Gbps multiplexers for optical transceivers. MOS Current Mode Logic (MCML) circuits allow much less output swing than conventional CMOS ones, and thus they can operate at a high frequency [1], [2].

As CMOS process technology scales, the power consumption of the circuit becomes large [3]. The power dissipation of MCML cells, which only is proportional to the product of their supply voltage and biasing current, are independent of their operation speed. Lowering supply voltage of MCML circuits would be a favourite technique to achieve low power-delay product (PDP) [4]. Therefore, the supply

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voltage of MCML circuits should be reduced as much as possible. On the other hand, MCML circuits are usually realized with dual-rail schemes [4]–[6]. However, the NMOS series structures in the dual-rail structure demand high enough supply voltage to ensure proper operating. Moreover, increased transistor counts because of dual-rail scheme result in extra area overhead [7]. The Single-Rail Current Mode Logic (SRCML) circuits have a smaller area overhead.

In CMOS processes, it is a main barrier against further scaling that the increasing leakage caused by short-channel effects and gate-dielectric leakage [8]. FinFETs (Fin-type Field-Effect Transistors) havs low leakage characteristic with excellent performance [9], [10]. Researches have been shown that FinFETs can offer remarkable advantages in terms of different design metrics [11]–[13]. On medium strong inversion regions, the FinFET devices provide stronger driving current than MOS ones. Therefore, it can be expected that FinFET current mode logic (FinFET CML) circuits can use a larger biasing current, and thus have more favourable performance than MCML ones. The previous research also indicates that multi-gate devices shows better parameter variation immunity than conventional bulk MOSFET.

In this work, a super-threshold computing scheme for FinFET SRCML circuits is addressed. The logic gates and a full-adder are implemented to verify the power efficiency. The two-input NAND based on FinFET SRCML, FinFET DRCML (Dual-rail Current Mode Logic), and static complementary FinFET logic are investigated in terms of probability distributions of propagation delay. All circuits are simulated with HSPICE at a PTM (Predictive Technology Model) 32 nm FinFET technology.

2. FinFET SRCML circuits

A single-rail edition of FinFET CML circuits is shown in Fig. 1, which is composed of three main parts: the P-type transistors P1 and P2 operating at linear region acted as resistors, the evaluation tree with full differential pull down switch network consisting of N1 and N2, and a biasing current source transistor Ns. The load resistors are adjusted by V_{rfp}, while the biasing current I_{B} is controlled by an added V_{rfn} [7].

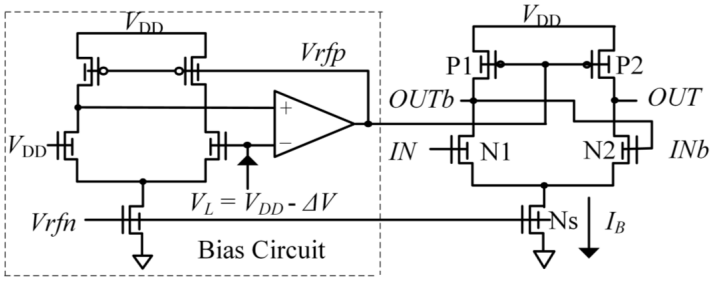

Fig. 1. FinFET SRCML inverter/buffer and its biasing circuit

The pull-down network switches the constant current between the left and right branches. The constant biasing current is converted to output voltage swing through

the two P-type load transistors. The high and low voltages of the outputs can be calculated $V_{\mathrm{OH}} = V_{\mathrm{DD}}$ and $V_{\mathrm{OL}} = V_{\mathrm{DD}} - I_{\mathrm{B}}R_{\mathrm{D}}$, respectively, where V_{DD} is source voltage, and R_{D} is the linear resistance of the P-type load transistors, respectively. The logic voltage swing can be written as $\Delta V = V_{\mathrm{OH}} - V_{\mathrm{OL}} = I_{\mathrm{B}}R_{\mathrm{D}}$. The proper logic swing ΔV is obtained by setting the negative-terminal voltage of the operational amplifier in the biasing circuits as $V_{\mathrm{L}} = V_{\mathrm{DD}} - \Delta V$, as shown in Fig. 1.

The structure of the FinFET SRCML circuits is simpler than the conventional dual-rail scheme, and thus it reduces area overhead. The power consumption can be expressed as

$$P = V_{\mathrm{DD}} \cdot I_{\mathrm{B}}\,. \tag{1}$$

The delay t_{d} of FinFET CML circuits can be expressed as

$$t_{\mathrm{d}} = 0.69RC = 0.69C(\Delta V/I_{\mathrm{B}})\,, \tag{2}$$

where C is the load capacitance of the output node in the MCML circuits. As is shown in (1), a direct solution for reducing power consumption is to lower the supply voltage. From (2), for given C and ΔV, if I_{B} is kept constant, the delay of FinFET CML circuits also keeps constant. Therefore, from (1), scaling supply voltage to super-threshold region can reduce power dissipation without performance degrading for a given I_{B}.

The FinFET SRCML circuits are realized only using an N-type transistor pull-down network to perform demanded logic operations. The logic functions of the 1-bit full adder can be expressed by the following formulas

$$Co = AB + Ci(B + A)\,, \tag{3}$$

$$S = ABCi + A\overline{BCi} + \overline{A}B\overline{Ci} + \overline{AB}Ci\,, \tag{4}$$

where A, B, Ci are input signal of the 1-bit full adder, Co is its carry output, and S is its sum. According to (3) and (4), it can be realized by using FinFET SRCML. Several logic styles have been used in the literature to design full adder cells. Each design style has its own merits and demerits. One example of such designs is the static conventional complementary logic FinFET full adder that is used for our comparisons of power and delay.

The total power consumption of static conventional complementary logic circuits can be expressed as

$$\mathrm{Ptotal} = \mathrm{Pdynamic} + \mathrm{Pstatic}\,, \tag{5}$$

where Pdynamic is dynamic power consumption, and Pstatic is leakage power consumption. Pdynamic can be specifically expressed as

$$\mathrm{Pdynamic} = C_{\mathrm{L}}V_{\mathrm{DD}}^2 f\,, \tag{6}$$

where C_{L} is the sum of all node capacitances and load capacitance in the full adder,

and f is the operating frequency. Pstatic can be expressed as

$$\text{Pstatic} = V_{\text{DD}} I_{\text{leakage}} , \tag{7}$$

where I_{leakage} is average leakage current. From (5), (6) and (7), the power dissipation of a static conventional circuit increases as its operating frequency. Considering the power consumption of FinFET CML circuits, therefore, there exists a frequency, known as the cross-frequency, above which the FinFET CML circuit is more power efficiency than the static one, and can be written as

$$f_{\text{c}} = \frac{I_{\text{B}} - I_{\text{leakage}}}{V_{\text{DD}} C_{\text{L}}} . \tag{8}$$

An optimization has been carried out for the FinFET SRCML and DRCML and traditional static complementary logic full adders. The power dissipation of three kinds of the full adders are compared in Fig. 2. As the operation frequency rises from 100 MHz to 3.2 GHz, the power dissipation of the traditional FinFET full adder increase rapidly, while the FinFET CML full adder keeps a constant value. Moreover, the power dissipation of FinFET SRCML full adder is slightly lower than FinFET DRCML full adder in various frequencies. The cross-frequency f_{c} is about 0.9 GHz. When the FinFET CML full adder operates at higher frequencies than 0.9 GHz, their power dissipation is lower than the traditional FinFET one.

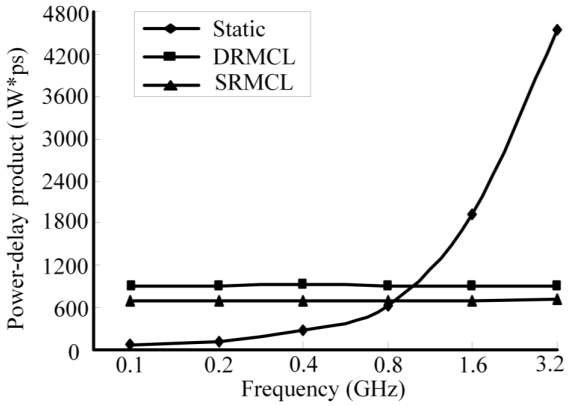

Fig. 2. Power dissipation comparisons of 1-bit full adders based on FinFET SRCML, DRCML and conventional static complementary logic in different operation frequencies

3. Super-threshold computing

A best solution for realizing power consumption of the FinFET CML circuits is to lower supply voltage. For a two-level FinFET SRCML circuit, as shown in Fig. 3, in order that the N-type FinFET transistor N1 operates at linear regions, the

minimum supply voltage is

$$V_{\mathrm{DD,min}} = V_{1,\mathrm{gs}} + V_{2,\mathrm{ds}} + V_{\mathrm{S,sat}} + \Delta V\,, \tag{9}$$

where $V_{1,\mathrm{gs}}$ is gate-source voltages of N1, $V_{2,\mathrm{ds}}$ is drain-source voltages of N2 when they operate in linear state, and $V_{\mathrm{S,sat}}$ is the drain-source voltage of Ns when it operates at saturation state. The first and second terms can usually be ignored. $V_{\mathrm{S,sat}}$ can be expressed as

$$V_{\mathrm{S,sat}} = \frac{I_{\mathrm{B}}}{2WC_{\mathrm{OX}}\nu_{\mathrm{sat}}} \times \left(\sqrt{1 + \frac{4E_{\mathrm{sat}}WLC_{\mathrm{OX}}\nu_{\mathrm{sat}}}{I_{\mathrm{B}}}} - 1\right), \tag{10}$$

where C_{OX}, ν_{sat}, and E_{sat} are unit oxide capacitance, saturation velocity, and saturation electric field, respectively, and W and L are effective width and length of transistors, respectively.

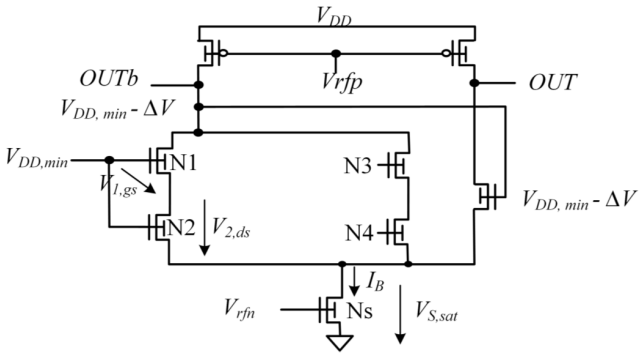

Fig. 3. Minimum operating supply voltage of FinFET SRCML circuits

According to (9) and (10), we can estimate the minimum supply voltage of FinFET SRCML circuits. We can lower its biasing current to reduce minimum supply voltage. If FinFET SRCML circuits operate at a low speed application, only a small bias current is required, and thus the supply voltage can be reduced, so that more energy saving can be realized. When FinFET CML circuits operate at a high speed application, a large bias current must be used, so that the minimum supply voltage must be increased.

The power consumption comparisons of the three kinds of 1-bit full adders with various supply voltages at 700 MHz is shown in Fig. 4. Scaling down the supply voltage can save power consumption effectively. The power consumption of the FinFET SRCML adder at 0.5 V and 0.8 V supply voltage is only 46.9 % and 79.9 % of 1.0 V supply voltage, respectively.

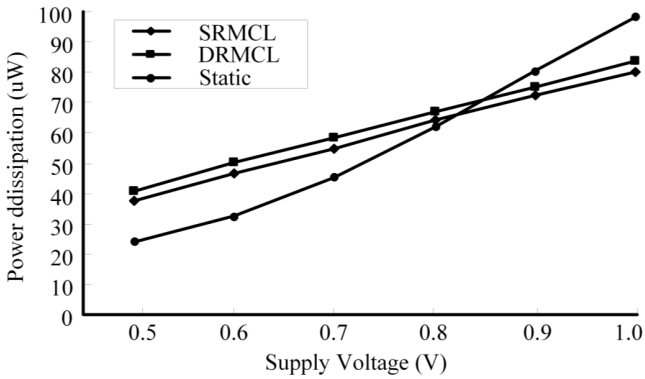

Fig. 4. Power consumption of the 1-bit full adder based on FinFET SRCML, DRCML and static logic in near-threshold and super-threshold regions

4. Performance variations

The requirement for very high-speed and low-power VLSI circuits is rapidly increasing. To improve the propagation delay, it is a perfect choice that sets a correct sizing of transistors as large W/L ratios make the switching fast. The performance variations of the circuits would make them must operate slowly. We have investigated the performance variations of various NAND2 based on FinFET SRCML, FinFET DRCML, and conventional static logic in terms of propagation delay (t_{p}). The Probability Density Function (PDF) of variability is calculated as the ratio of standard deviation (σ) to mean value (μ) of any design metric.

Monte Carlo simulation is carried out for 10 % variations in threshold voltage V_{th}, channel width W, channel length L, and oxide thickness t_{ox}. The delay variability is observed in the source voltage from 950 mV to 750 mV, shown in Fig. 5. The voltage swing of FinFET CML circuits ΔV is 0.3 V. PDF is estimated with 250 sample sizes to achieve high accuracy.

It can be clearly noted that static logic NAND2 is more prone to variations than FinFET CML, because the conventional static logic structure has symmetric structure. Therefore, FinFET CML circuits are established as robust circuits, and appear to have higher immunity against voltage and process variations.

The variability (σ/μ) of NAND2 based on FinFET SRCML always keeps larger than FinFET DRCML circuits with various source voltages. The FinFET DRCML NAND2 has stronger robustness against variations than FinFET SRCML, because the differential symmetry structure of FinFET SRCML is slightly broken although it is simpler than the dual-rail ones.

In super-threshold region, the PDF (σ/μ) of NAND2 based on FinFET DRCML circuits almost keeps a constant about 1.60 %, which is much less than ones in near-threshold region. However, the PDF (σ/μ) of NAND2 based on FinFET SRCML circuits almost keeps a constant in both super-threshold and near-threshold regions.

The simulated outcomes of variability analysis of FinFET SRCML NAND2 are shown in Fig. 6 in term of t_{p}. From (2), for given I_{B} and ΔV, because between t_{d} and

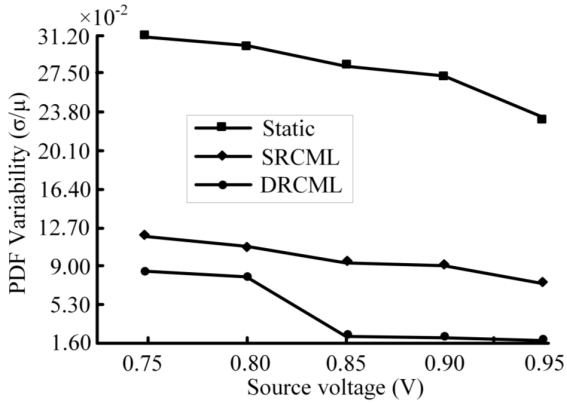

Fig. 5. PDF variability comparison of NAND2 circuit based on FinFET SRCML, DRCML, and conventional static logic

C there exists a linear relationship, and the standard deviation of C keeps constant, the delay standard deviation of FinFET SRCML circuits also keeps constant, about 26.28 ps as shown in Fig. 6. The PDF of the FinFET SRCML AND2 gate, normalized to the standard deviation as a function of V_{DD} is also shown in Fig. 6. At $V_{\mathrm{DD}} = 0.95\,\mathrm{V}$, the PDF is substantially Gaussian, while it is non-Gaussian at $V_{\mathrm{DD}} = 0.75\,\mathrm{V}$.

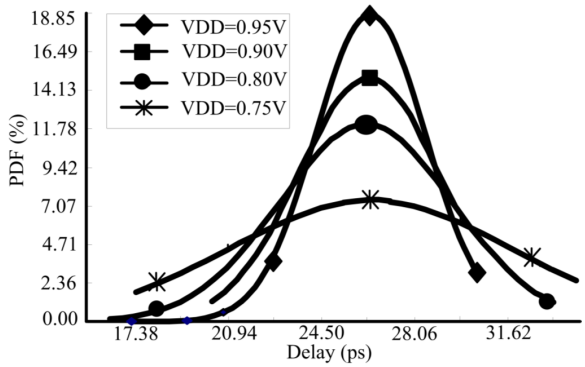

Fig. 6. PDF of stochastic delays of the FinFET SRCML AND2 gate by the corresponding standard deviation with various source voltages

5. Conclusion

Scaling down the supply voltage of FinFET SRCML circuits can effectively reduce their power consumption, because their power dissipation is in direct proportion to the supply voltage. However, the supply voltage of the FinFET SRCML circuits has a minimum limit for ensuring the proper operation. In this paper, a super-threshold

computing scheme for FinFET SRCML circuits has been addressed to attain low power dissipation. The super-threshold FinFET SRCML circuits can realize faster operation than near-threshold one, since the larger biasing current can be used. The relationship between the minimum supply voltage and the model parameters of FinFET transistors has been derived, so that the optical supply voltage of FinFET SRCML circuits can be estimated before circuit designs.

A full-adder has been implemented to verify the power efficiencies. The power consumption of FinFET SRCML circuits can be reduced by lowering the supply voltage to super-threshold regions without performance degrading and accepted performance variation penalty.

FinFET SRCML has a slightly weak robustness against variations compared with FinFET DRCML, but it has better robustness against variations than conventional static logic. As the source voltage is reduced, the delay standard deviation of FinFET SRCML circuits almost keeps constant.

References

[1] J. Hu, H. Ni, Y. Xia: *High-speed low-power MCML nanometer circuits with near-threshold computing.* Journal of Computers *8* (2013), No. 1, 129–135.

[2] J. M. Musicer, J. Rabaey: *MOS current mode logic for low power low noise CORDIC computation in mixed-signal environments.* Proc. IEEE International Symposium on Low Power Electronics and Design, 26–27 July 2000, Rapallo, Italy, 102 to 107.

[3] J. Hu, X. Yu: *Low voltage and low power pulse flip-flops in nanometer CMOS processes.* Current Nanoscience *8* (2012), No. 1, 102–107.

[4] Y. Wu, J. Hu: *Low-voltage MOS current mode logic for low-power and high speed applications.* Information Technology Journal *10* (2011), No. 12, 2470–2475.

[5] M. Alioto, G. Palumbo: *Design strategies for source coupled logic gates.* IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications *50* (2003), No. 5, 640–654.

[6] H. Hassan, M. Anis, M. Elmasry: *MOS current mode circuits: analysis, design, and variability.* IEEE Transactions on Very Large Scale Integration (VLSI) Systems *13* (2005) No. 8, 885–898.

[7] H. Li, R. Cao, J. Hu: *Single-rail MOS current mode logic circuits for low-power and high-speed applications.* Advances in Information Sciences and Service Sciences(AISS) *4* (2012), No. 22, 27–36.

[8] Y. Wu, J. Hu, Y. Zhang: *Super-threshold FinFET full adders for low-power and high-speed applications.* Electrotehnica, Electronica, Automatica *63* (2015), No. 1, 97 to 104.

[9] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, C. Hu: *Sub 50-nm FinFET: PMOS.* Proc. IEEE International Electron Devices Meeting, 5–8 Dec. 1999, Washington, DC, USA, 67–70.

[10] M. Agostinelli, M. Alioto, D. Esseni, L. Selmi: *Leakage–delay tradeoff in FinFET logic circuits: A comparative analysis with bulk technology.* IEEE Transactions on Very Large Scale Integration (VLSI) Systems *18*, (2010), No. 2, 232–245.

[11] F. He, X. Zhou, C. Ma, J. Zhang, Z. Liu, W. Wu, X. Zhang, L. Zhang: *FinFET: From compact modeling to circuit performance.* IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), 5–17 Dec. 2010, Hong Kong, China, 1–6.

[12] E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C. Chuang, K. Bernstein, R. Puri: *Turning silicon on its edge [double gate CMOS/FinFET technology.* IEEE Circuits and Devices Magazine *20* (2004), No. 1, 20–31.

[13] X. Zhang, J. Hu, X. Luo: *Optimization of dual-threshold independent-gate FinFETs for compact low power logic circuits.* Proc. IEEE International Conference on Nanotechnology (IEEE-NANO), 22–25 Aug. 2016, Sendai, Japan, IEEE Conference Publications (2016), 529–532.

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